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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,408	10/08/2003	Leonard Forbes	400.250US01	7405

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,408	FORBES, LEONARD	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date May 18, 2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1A, 1B, 1C and 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Fastow et al. (U.S. Pat. No. 6,583,479).

Regarding claim 1, Fastow et al. disclose a vertical multiple bit cell (see figures 8-9), comprising: a vertical metal oxide semiconductor field effect transistor (MOSFET) extending outwardly from a substrate (memory cells 822, 824 extending outwardly from a substrate 802), the MOSFET having a first source/drain region (first source/drain region 804), a second source/drain region (second source/drain region 806, 808 for cells 822, 824), a channel region (channel region 828 for cell 822 and channel region 830 for cell 824) between the first and the

second source/drain regions (channel region 828, 830 between the first source/drain region 804 and second source/drain region 806, 808 for cells 822, 824, respectively), and a gate separated from the channel region by a high dielectric constant gate insulator that can store a first charge in a first storage region and a second charge in a second storage region (gate 816, 818 of cells 822, 824 separated from the channel region 828, 830 by a high dielectric constant gate insulator (ONO layer) 810, 812, 814) that can store a first charge in a first storage region and a second charge in a second storage region); a first transmission line coupled to the first source/drain region (contact 820 for connecting charge to the first source/drain region 804 by a conductor line); a second transmission line coupled to the second source/drain region (contact 826 for connecting the second source/drain region 806, 808 by a conductor line; col. 13, lines 60+; col. 4, lines 55+).

Regarding claim 2, Fastow et al. disclose the multiple bit cell of claim 1, wherein the substrate is coupled to a negative bias that enhances hot electron injection (negative charge is normally applying to the substrate of the memory cell transistor to enhance the electron injection to the tunnel region and to improve the breakdown bias to the substrate).

Regarding claim 3, Fastow et al. disclose a vertical multiple bit cell as of claim 1 wherein the MOSFET is operated with either the first source/drain region or the second source/drain region serving as the source region in response to a direction of operation of the MOSFET (source/drain regions of the memory cell transistor are interchangeable and the cell bit is stored to which direction responding to the source or drain side of the memory cell, col. 4, line 55+).

Regarding claims 4-5, Fastow et al. disclose a vertical multiple bit cell of claim 1 wherein the MOSFET includes the first and second charges simultaneously programmed into both the

first and second storage regions (first and second charges simultaneously programmed into both the first storage region adjacent to first source/drain region and second storage region adjacent to second source/drain region; lines 60+; col. 4, lines 55+).

Regarding claim 6, Fastow et al. disclose a vertical multiple bit cell of claim 1 wherein the gate insulator includes a composite layer of oxide-nitride-aluminum oxide (col. 14, lines 29+; col. 2, lines 55+).

Regarding claim 7, Fastow et al. disclose a vertical multiple bit cell of claim 1 wherein the gate insulator is comprised of two or more oxide materials selected from the group of silicon, titanium, tantalum, hafnium, and lanthanum (col. 14, lines 29+; col. 2, lines 55+).

Claims 8-15 claiming the similar limitation as previously discussed in claims 1-7. Therefore, they are analyzed as previously discussed with respect to claims 1-7.

Claims 20-23 claiming the method of forming the structure of the device as previously discussed in claims 1-15. Therefore, the method as claimed is met by the structure for the cited device.

Regarding claims 16-19, the apparatus as previously discussed in claims 1-15 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-15.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-64 of copending Application No. 10/177,208. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are claiming the same scope of the invention claiming the vertical multiple bit memory cell extending outwardly from substrate.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
October 1, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818